Notice of Allowability	Application No.	Applicant(s)	
	10/603,797	HONMURA, TETSUROO	
	Examiner	Art Unit	
	Tanh Q. Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *February 6, 2007*.

2. ☒ The allowed claim(s) is/are *5-16*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 13, 2006 has been entered. Additionally, applicant's supplemental submission filed on February 6, 2007 (to correct minor errors in claims 5 and 7) has also been entered.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with the attorney for applicant, Larry Anagnos (Reg. No. 32,392) on April 25, 2007 to incorporate allowable subject matter and to correct minor informalities - in order to put the application in condition for allowance.

The application has been amended as follows:

5. (Currently Amended) A semiconductor integrated circuit device comprising:

a CPU related to a first memory space;

a peripheral LSI related to a second memory space;

a CPU bus connected between the CPU and the peripheral LSI and related to the first memory space; and

an I/O bus connected to the peripheral LSI and related to the second memory space;

wherein the peripheral LSI comprises:

an address translation circuit;

a nonvolatile memory to store address information indicating a relationship between an address of the first memory space and an address of the second memory space; ~~and~~

a CODEC circuit to compress and uncompress video data;

a first protocol decode and generation circuit connecting to a first bus connected to the first memory space; and

a second protocol decode and generation circuit connecting to a second bus connected to the second memory space;

wherein the address translation circuit is connected to the first and second protocol decode and generation circuits and comprises:

a register, and

an address calculation circuit,

wherein, when the semiconductor integrated circuit device is initialized, the register reads the address information from the nonvolatile memory;

wherein, when the CPU acts as a bus master to access the second memory space, the first protocol decode and generation circuit receives a first address in the first memory space and sends the first address to the address calculation circuit, the address calculation circuit translates the first address into a second address in the second memory space from the address information stored in the register, and the address calculation circuit sends the second address to the second protocol decode and generation circuit;

wherein, when the peripheral LSI acts as a bus master to access the first memory space, the second protocol decode and generation circuit receives a third address in the second memory space and sends the third address to the address calculation circuit, the address calculation circuit translates the third address into a fourth address in the first memory space from the address information stored in the register, and the address calculation circuit sends the fourth address to the first protocol decode and generation circuit; ~~and~~

wherein the CODEC circuit in the peripheral LSI receives compressed first video data from the CPU bus, uncompresses the compressed first video data into uncompressed first video data, and transfers the uncompressed first video data to the I/O bus;

wherein the CODEC circuit in the peripheral LSI receives second video data from

the I/O bus, compresses the second video data into compressed second video data, and transfers the compressed second video data to the CPU bus; and

wherein the semiconductor integrated circuit device further comprises:

a first memory;

a second memory;

a flash memory; and

an LCD controller;

wherein the first memory and the flash memory are connected to the CPU bus; and

wherein the second memory and the LCD controller are connected to a camera

~~wherein the uncompressed video data is transferred through the peripheral LSI from the CPU bus to the I/O bus after the CODEC circuit uncompresses the compressed video data; and~~

~~wherein the compressed video data is transferred through the peripheral LSI from the I/O bus to the CPU bus after the CODEC circuit compresses the video data~~.

6. (Previously Presented) The semiconductor integrated circuit device according to claim 5, wherein the address information is stored in the nonvolatile memory when a probing test is conducted on the semiconductor integrated circuit device.

7. (Currently Amended) A semiconductor integrated circuit device comprising:

a CPU related to a first memory space;

a peripheral LSI related to a second memory space;

a CPU bus connected between the CPU and the peripheral LSI and related to the first memory space; and

an I/O bus connected to the peripheral LSI and related to the second memory space;

wherein the peripheral LSI comprises:

an address translation circuit;

a nonvolatile memory; ~~and~~

a CODEC circuit to compress and uncompress video data;

a first protocol decode and generation circuit connecting to a first bus connected to the first memory space; and

a second protocol decode and generation circuit connecting to a second bus connected to the second memory space;

wherein the address translation circuit is connected to the first and second protocol decode and generation circuits and comprises:

a register, and

an address calculation circuit,

wherein the nonvolatile memory stores a first start address in a first memory range belonging to the first memory space and a second start address in

a second memory range belong to the second memory space;

wherein the second memory range is allocated to the first memory range;

wherein, when the semiconductor integrated circuit device is initialized, the register reads the first start address and the second start address from the nonvolatile memory;

wherein, when the CPU acts as a bus master to access the second memory space, the first protocol decode and generation circuit receives a first address in the first memory space and sends the first address to the address calculation circuit, the address calculation circuit translates the first address into a second address in the second memory space from the address information stored in the register, and the address calculation circuit sends the second address to the second protocol decode and generation circuit;

wherein, when the peripheral LSI acts as a bus master to access the first memory space, the second protocol decode and generation circuit receives a third address in the second memory range and sends the third address to the address calculation circuit, the address calculation circuit translates the third address into a fourth address in the first memory range from the first start memory address, the second start memory address, and the third address which are stored in the register, and the address calculation circuit sends the fourth address to the first protocol decode and generation circuit, ~~and~~

wherein the CODEC circuit in the peripheral LSI receives compressed first video data from the CPU bus, uncompresses the compressed first video data into

uncompressed first video data, and transfers the uncompressed first video data to the I/O bus;

wherein the CODEC circuit in the peripheral LSI receives second video data from the I/O bus, compresses the second video data into compressed second video data, and transfers the compressed second video data to the CPU bus; and

wherein the semiconductor integrated circuit device further comprises:

a first memory;

a second memory;

a flash memory; and

an LCD controller;

wherein the first memory and the flash memory are connected to the CPU bus; and

wherein the second memory and the LCD controller are connected to a camera

~~wherein the uncompressed video data is transferred through the peripheral LSI from the CPU bus to the I/O bus after the CODEC circuit uncompresses the compressed video data; and~~

~~wherein the compressed video data is transferred through the peripheral LSI from the I/O bus to the CPU bus after the CODEC circuit compresses the video data~~.

8. (Previously Presented) The semiconductor integrated circuit device according to claim 7:

wherein the address calculation circuit translates the third address into the fourth

address ~~from a formula: the first start address + the third address - the second start address~~ by adding the first start address to the third address and subtracting the second start address.

9. (Previously Presented) The semiconductor integrated circuit device according to claim 7:

wherein the nonvolatile memory further stores a first address width of the first memory range;

wherein the address translation circuit further comprises an address selection circuit and an interrupt circuit;

wherein, when the ~~semiconductor integrated circuit~~ peripheral LSI acts as a bus master to access the first memory space, the address selection circuit decides whether or not the first address belongs to the second memory range; and

wherein the address selection circuit outputs an error signal if the first address ~~doesn't~~ does not belong to the second memory range.

10. (Previously Presented) The semiconductor integrated circuit device according to claim 7:

wherein the nonvolatile memory stores a third start address in a third memory range belonging to the ~~second~~ first memory space and a fourth start address in a fourth memory range belonging to the ~~first~~ second memory space;

wherein the fourth memory range is allocated to the third memory range;

wherein, when the semiconductor integrated circuit device is initialized, the register reads the third start address and the fourth start address from the nonvolatile memory; and

wherein, when a second CPU acts as a bus master to access the second memory space, the first protocol decode and generation circuit receives a fifth address in the ~~first~~ third memory range and sends the fifth address to the address calculation circuit, the address calculation circuit translates the fifth address into a sixth address in the fourth memory range from the third start memory address, the fourth start address, and the fifth address which are stored in the register, and the address calculation circuit sends the sixth address to the second protocol decode and generation circuit.

11. (Previously Presented) A semiconductor integrated circuit device according to claim 5, wherein the address translation circuit is part of a flexible bus controller which is separate from the CPU.

12. (Previously Presented) A semiconductor integrated circuit device according to claim 7, wherein the address translation circuit is part of a flexible bus controller which is separate from the CPU.

13. (Previously Presented) A semiconductor integrated circuit device according to claim 11, wherein said flexible bus controller further comprises said first and second protocol decode and generation circuits.

14. (Previously Presented) A semiconductor integrated circuit device according to claim 12, wherein said flexible bus controller further comprises said first and second protocol decode and generation circuits.

15. (Previously Presented) A semiconductor integrated circuit device comprising:

a CPU related to a first memory space;

a peripheral LSI related to a second memory space;

a CPU bus connected between the CPU and the peripheral LSI and related to the first memory space; and

an I/O bus connected to the peripheral LSI and related to the second memory space;

wherein the peripheral LSI is ~~LSI, is~~ separate from the first CPU, and is adapted to transfer data between said first CPU and a peripheral device, said peripheral LSI comprising:

an address translation circuit;

a nonvolatile memory to store address information indicating a relationship between an address of the first memory space and an address of the second memory space;

a CODEC circuit to compress and uncompress video data;

a first protocol decode and generation circuit connecting to a first bus

connected to the first memory space; and

a second protocol decode and generation circuit connecting to a second bus connected to the second memory space;

wherein the address translation circuit is connected to the first and second protocol decode and generation circuits and comprises:

a register, and

an address calculation circuit,

wherein, when the CPU acts as a bus master to access the second memory space, the first protocol decode and generation circuit receives a first address in the first memory space and sends the first address to the address calculation circuit, the address calculation circuit translates the first address into a second address in the second memory space from the address information stored in the register, and the address calculation circuit sends the second address to the ~~first~~ second protocol decode and generation circuit;

wherein the CODEC circuit in the peripheral LSI receives compressed first video data from the CPU bus, uncompresses the compressed first video data into uncompressed first video data, and transfers the uncompressed first video data to the I/O bus;

wherein the CODEC circuit in the peripheral LSI receives second video data from the I/O bus, compresses the second video data into compressed second video data, and transfers the compressed second video data to the CPU bus; and

wherein the semiconductor integrated circuit device further comprises:

a first memory;

a second memory;

a flash memory; and

an LCD controller;

wherein the first memory and the flash memory are connected to the CPU bus; and

wherein the second memory and the LCD controller are connected to a camera

~~wherein the uncompressed video data is transferred through the peripheral LSI from the CPU bus to the I/O bus after the CODEC circuit uncompresses the compressed video data; and~~

~~wherein the compressed video data is transferred through the peripheral LSI from the I/O bus to the CPU bus after the CODEC circuit compresses the video data~~.

16. (Previously Presented) A semiconductor integrated circuit device according to claim 15, wherein the peripheral LSI further comprised a flexible bus controller which includes said address translation circuit and said first and second protocol decode and generation circuits.

Cancel claims 17-19.

Allowable Subject Matter

3. The following is an examiner's statement of reasons for allowance: The prior art, individually or in combination, does not teach the elements of the semiconductor integrated circuit device being connected and functioning in the manner claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Q. Nguyen whose telephone number is 571-272-4154. The examiner can normally be reached on M-F 9:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TANH Q NGUYEN
PRIMARY EXAMINER
TECHNOLOGY CENTER 2100

April 26, 2007

TQN
April 26, 2007